© CSVTU Research Journal on Engineering and Technology: Swami Vivekanand Technical University All Rights Reserved.

CSVTU Research Journal on Engineering and Technology
Vol. 8(1), 31–38, 2019 ISSN: 0974-8725

A Review Article on Fin Field Effect Transistors Technology

Nidhi Dhurandhar* and Prashant Dwivedi

Department of Microelectronics and VLSI,
Chhattisgarh Swami Vivekanand Technical, University, Newai, Pin-491107, Chhattisgarh, India
*Corresponding author, E-mail: dhurandharnidhi@gmail.com

Received June 26 2019; received in revised form July 25, 2019; accepted July 25 2019; Available online July2019

Research Article

Abstract

There are numerous types of transistors present in electronics domain. Beyond them, here, this paper discusses an exhaustive type of Metal Oxide Field Effect Transistor (MOSFET), that is, Fin Field Effect Transistor (FinFET). In today's era FinFET Technology is in great demand and is very prominent type of Field Effect Transistor that allows highly controllable and fast execution of transistor applications and simulation, both in digital and analog domains. Moore's law says the number of transistors implemented on a single Integrated Circuit (IC) gets doubled every two year. So the transistor sizing became an important key to fulfill the desired applications requirement. But CMOS transistor size can be minimized up to some limits and beyond that the gate loses its control over channel and causing an issue called as Short Channel Effect (SCE). To overcome this issue and to improve the execution and power capability of the semiconductor applications, FinFET has been implemented. In this review paper, different type of FinFET structures and their classifications along with some digital circuits design examples has been discussed.

***Keywords**:* FinFET, SCE, Independent Gate FinFET, Short Gate FinFET, Asymmetric Short Gate FinFET, Static Random Access Memory (SRAM).

1. Introduction

Since we all know that the semiconductor industry is growing and developing day by day. Moore's law says the total transistors density implemented on a single Integrated Circuit (IC) gets doubled every two year. So, the transistor size must be reduced to achieve the desired applications of a chip [1]. But transistor sizing can be done up to some limits and by minimizing the channel length beyond certain limit makes the gate to lose its control over the channel, which causes Short Channel Effects (SCE) [2] and this can affect device performance and conductivity [1]. Due to SCEs performance of the device are degraded makings the device incompatible [3] below 20 nanometers [2]. To upgrade the gate controllability over a channel, semiconductor industry has switched to a different FET that is Fin Field Effect Transistor (FinFET). It is mostly a MOSFET fabricated over a bulk or SOI substrate. It is having its gate to be fabricated over two, three sides or all around the channel to form a multi gate structure. FETs are called "FinFET" because its source and drain regions make fins on the Si surface [4]. They are also called as i.e., Multi-Gate FET (MGFET) [5].

Though these MGFET's have unrestrained nature over random doping and over minimal parasitic capacitances, they are more advantageous than classical CMOS structures [6]. Since the tri gate FETs has minimal edge capacitances but the fabrication process cost is much higher due to its highly complicated structure [3]. During the designing of dynamic circuits, noise becomes a major issue. The prospect of logical failure is enlarged because of the weak noise tolerance of dynamic circuits [7]. To overcome this issue, FinFET is implemented, which has enhanced controllability over a channel for low power specifications which enhances its noise tolerance [8].

There are various advantages of FinFET over bulk MOSFET, one is a better voltage gain. FinFET has two or three times higher voltage gain alongside MOSFET [9]. These FETs are also having more enhanced electrical coupling properties in between the back and front transistor. They also provide innovative circuit specifications because of their two fold structure [9]. Since the conventional MOSFETs does not have better controllability of gate over the channel and cannot tolerate the noise injection under 32nm technology so this new improved technology has been introduced.

2. Process technology

This section gives a detailed description on FinFET Technology and gives a brief overview about various FinFET structure types, their need and classifications in detail. The main reason for higher desirability of FinFET over the past decennary period is the indignity of SCEs alongside bulk MOSFETs. In Figure 1, we can see the graphical representation of Drain-Induced Barrier Lowering (DIBL) and channel length for Double-Gate (DG), to manifest the fulfillment of SCEs of FinFET over bulk MOSFETs having the same channel length. Figure 2 shows the comparison of planar MOSFET and FinFET [10].

Though the bulk MOSFET has a parallel channel, FinFET has the multiple perpendicular channels which look like 'fin' of a fish so is termed as "fin".

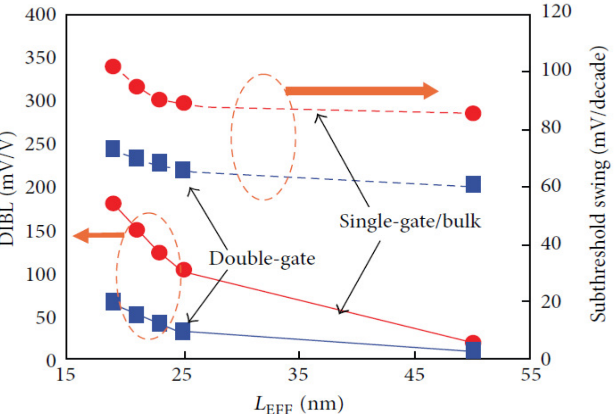


Figure 1 DIBL and Sub-threshold Swing (S) versus effective channel length for DG and bulk-silicon nFETs.

Because of this 'fin' structure the channel height regulates the FET's width (W)[11]. According to "width quantization" property which says "the width of FinFET is multiple of the height of the fin" thus the width can be inflated by the use of several fins. Because of this, random FinFET widths can't be possible. The DG device is designed with an undoped body and a near-mid-gap gate material [Courtesy to Reference 10].

We can enhance the drive current of FinFET by enhancing the channel's width, that is, by enhancing the fin's height. The drive current can also be enhanced by manufacturing several parallel fins which are coupled together. The classifications and effective

channel length are described in below section.

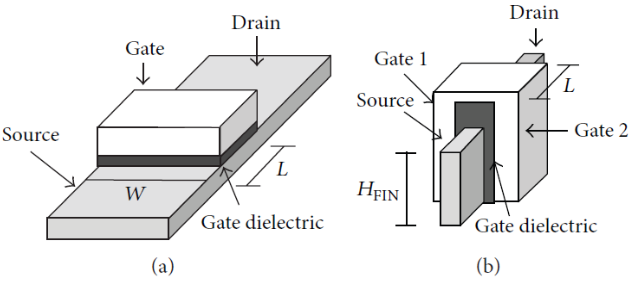


Figure 2 Structural comparison between (a) planar MOSFET and (b) FinFET [Courtesy to Reference 10].

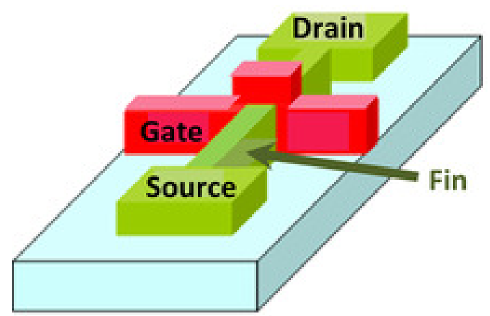


Figure 3 FinFET Structure [Courtesy to Reference 4].

2.1 Classifications: The FinFETs are classified in basically two categories:

(i) Independent Gate FinFET (IGF).
(ii) Short Gate FinFET (SGF).
Table 1 shows the comparison between Independent Gate FinFET (IGF) and Short Gate FinFET (SGF). By using SGF, a 6T SRAM is designed in Figure 4.
We generally prefer SGF over IGF because of its cheaper price, less area consumption and better on and off currents. Short Gate FinFETs are also designated cased on device parameter's asymmetric. This SGF is also named Asymmetric Short Gate FinFET (ASGF). Figure 5 shows the structure of ASG FinFET that can be manufactured by using two different dopants to fabricate two types of gate stacks (shorted gates but are of different dopants) [10].

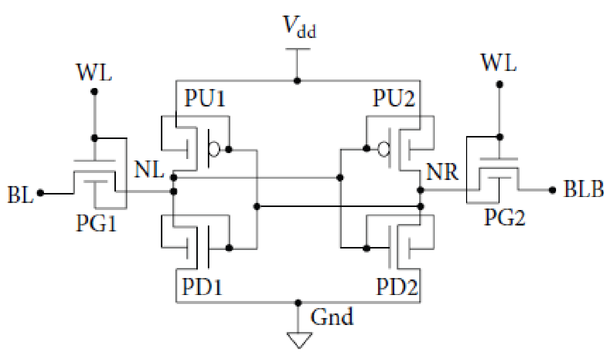


Figure 4 Schematic design of 6-T SRAM cell using SGF [Courtesy to Reference 10]

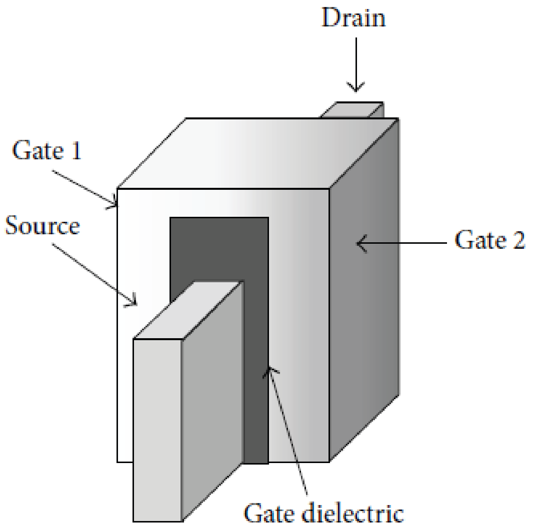


Figure 5 Structure of ASG FinFET; shaded gate implies different work functions [Courtesy to Reference 10].

Generally, both gates of this FinFET have the same work functions (Φ) but they came be changed too [10]. Figure 6 and 7 shows Drain current (*IDS*) versus front-gate voltage (*VGFS*) for three nFinFETs [10]; and Drain current (*IDS*) versus front-gate voltage (*VGFS*) for three pFinFETs [10] respectively to reveal the advantages of ASGF.

Table 1Comparison between IGF and SGF

IGF	**SGF**
1. Structure of IGF [Courtesy to Reference 10].	1. Structure of SGF [Courtesy to Reference 10].
2. IG FinFETs are also known as four terminal FinFETs [3].	2. SG FinFETs are also known as three terminal FinFETs [3].
3. IGFs have the substantially unaccompanied gates (that are not connected) [3].	3. SGFs are having substantially shorted gates (both the back and front gates are combined together) [3].
4. On the other hand, IGFs provides better flexibility of application of different inputs to different gates. But that makes it more expensive because of larger chip area consumption [3].	4. Due to combined gates, SGFs offers excessive on and off-currents (subthreshold currents and Ioff) respectively in comparison with IGFs. SGFs also provide better control over electrostatics of channel [3].

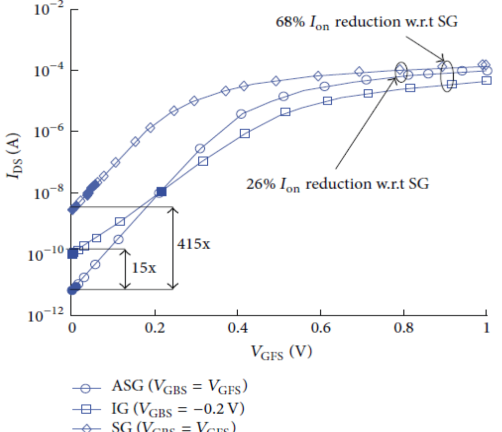


Figure 6 Drain current (*I*DS) versus front-gate voltage (*V*GFS) for three nFinFETs of ASGF [Courtesy to Reference 10]

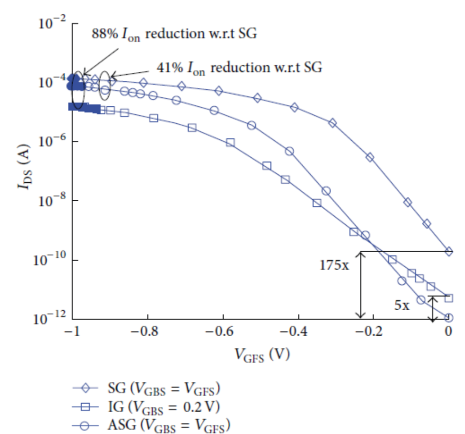


Figure 7 Drain current (*I*DS) versus front-gate voltage (*V*GFS) for three pFinFETs of ASGF [10]

2.2 Schematic Diagrams:

2.2.1 n-FinFETs and p-FinFETs: In Figure 8 we can see the n-FinFETs using SGF and IGF having work function of 4.4eV [10].

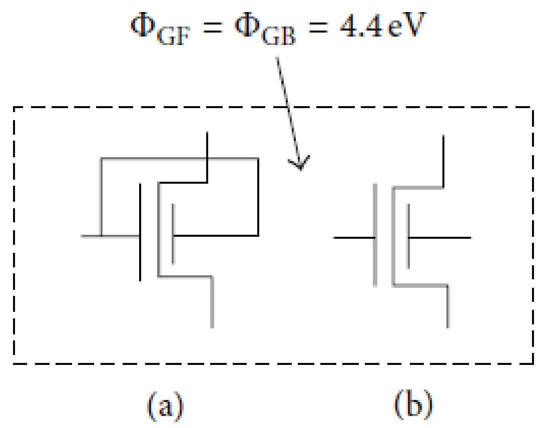


Figure 8 Schematic diagram of n-FinFET (a) using SGF and (b) using IGF [Courtesy to Reference 10].

Similarly, Figure 9 shows the p-FinFETs using SGF and IGF having work function of 4.8Ev [10]. And Figure 10 shows the n-FinFET and p-FinFET using ASGF having the work function of 4.4Ev [10].

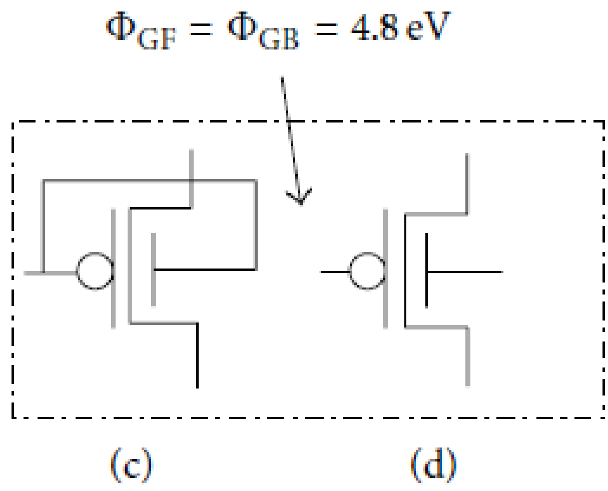


Figure 9 Schematic diagram of p-FinFET (c) using SGF and (d) using IGF [Courtesy to Reference 10].

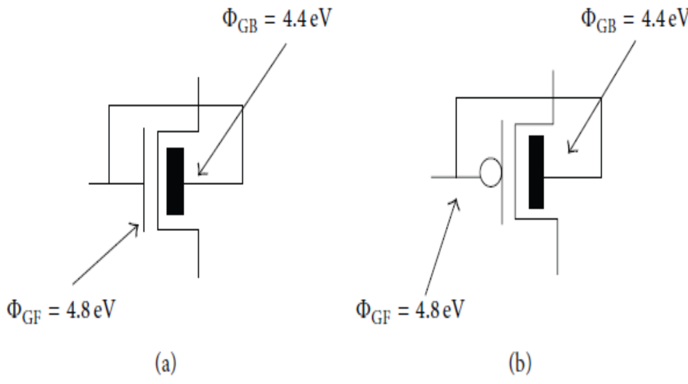


Figure 10 Schematic diagram of (a) n-FinFET and (b) p-FinFET using ASGF [Courtesy to Reference 10].

2.2.2 Inverters: Figure 11 shows the schematic diagram of inverter using SGF and IGF respectively and Figure 12 shows inverter using ASGF.

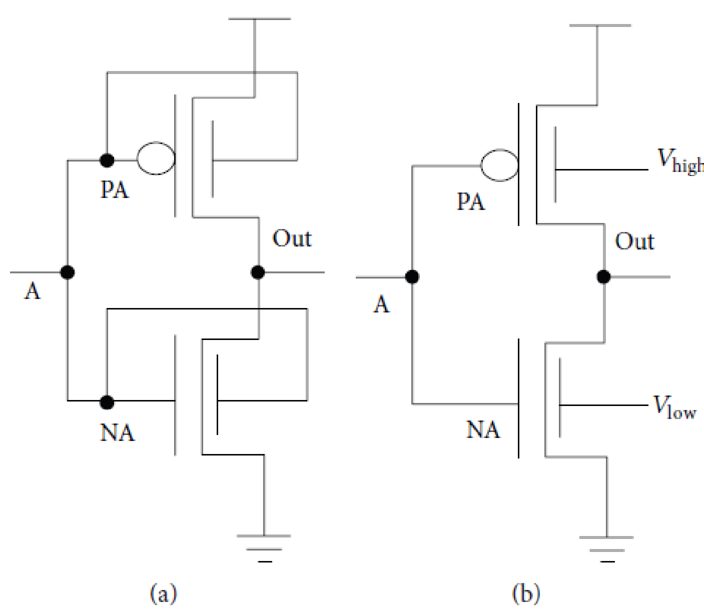


Figure 11 Schematic diagram of inverter using (a) SGF and (b) using IGF [Courtesy to Reference 10].

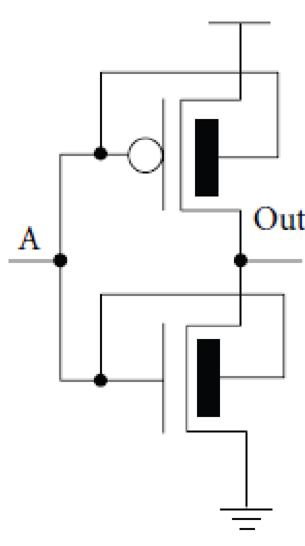
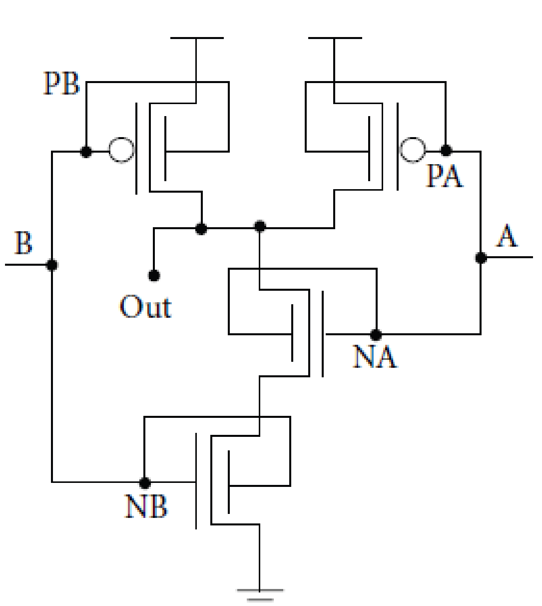


Figure 12 Schematic diagram of inverter using ASGF [Courtesy to Reference 10].

2.2.3 Two-inputs NAND gates: In Figure 13, we can see the schematic diagram of two-inputs NAND gate using SGF and IGF respectively and in Figure 14, we can see NAND gate using ASGF.

(a)



(b)

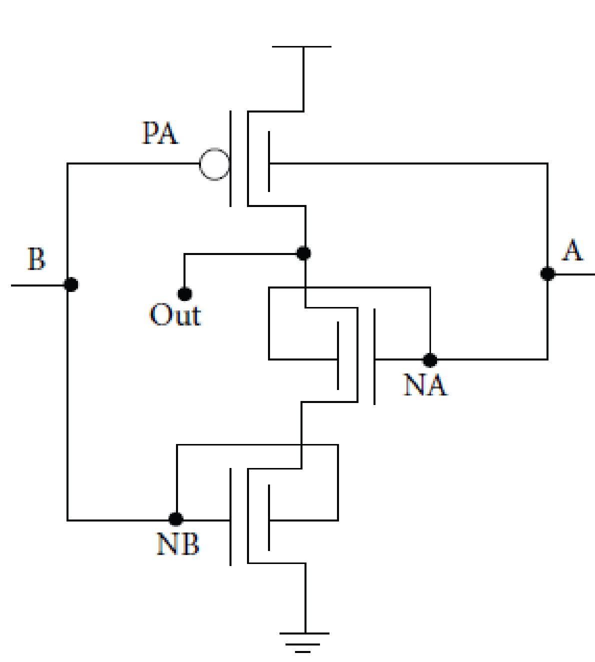


Figure 13 (a)-(b) Schematic diagram of two-inputs NAND gates using SGF (left side) and IGF (right side) [Courtesy to Reference 10].

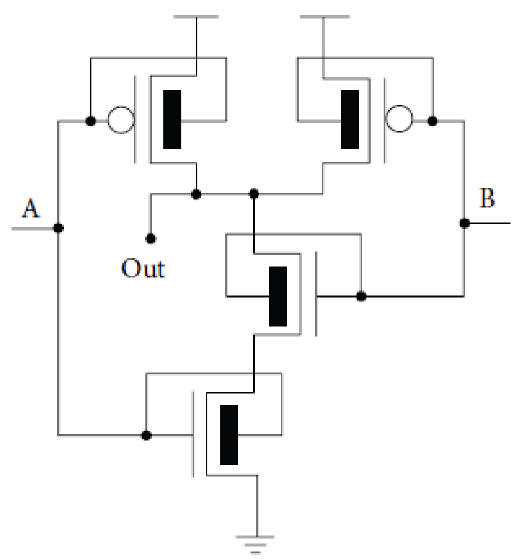


Figure 14 Schematic diagram of two- inputs NAND gate using ASGF [Courtesy to Reference 10].

3. Problem identification

In this section, we will see some drawbacks of FinFETs that we have identified during this review. Below are the listed problems occurred in FinFETs and they are as under:

3.1 Gate Patterning: While patterning the fin of FinFET, the gate must be compacted, which is toughest part in case of FinFET because the gate is wrapped around the channel or some FinFETs have multiple gates which is tough to design. Figure 15 shows the critical gate patterning [12].

3.2 Parasitic Resistance: As the width if fin (Wfin) is scaled down, one parasitic resistance i.e., RSD (Source-Drain Resistance) occurs, which becomes a major issue now. Since to control the SCEs, the fins of FinFET must be narrow. But because of this, the degradation of parasitic RSD is critical [13].

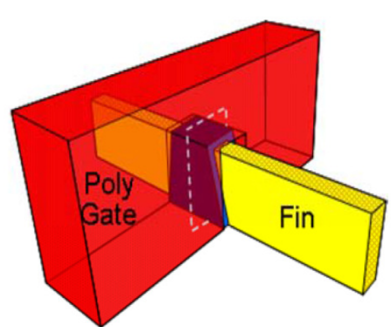


Figure 15 Critical gate patterning step with a risk of a tapered gate profile with poly/MG/high-k gate stack [Courtesy to Reference 12].

3.3 Issue occurring during doping: Since FinFET needs a very concise and minimized structure and has multiple fins too so a major fabrication issue occurs due to the need of highly accurate and low resolution structure fabrication. One advanced and matured technique for fulfilling this constrains is Ion Implantation. But there is also one major issue with ion implantation technique is that it has its angle restriction which is mandatory to avoid shadowing while implantation of dense structures [13].

4. FUTURE SCOPE

There are some recommendations for future work are listed in this section:

- The more concise and matured technique should be proposed to eliminate the parasitic resistances.
- The gate should be implemented and fabricated by using more advanced techniques.
- The doping technique should be improved.

Conclusion

In this review article, we have seen the basic overview of FinFET which is implemented to overcome the SCEs that occurs in MOSFETs. Then we had a look over FinFET classifications and some schematic structures of gates by using different type of FinFETs. The issues occurring in FinFET and some scopes to eliminate those have been discussed successfully.

Acknowledgment

The authors are thankful to Chhattisgarh Swami Vivekanand Technical University (CSVTU), Bhilai to provide such a precious opportunity to study and successfully execution of the work.

Conflict of Interest

The authors declare no conflict of interest.

References

1. Taur Y. and Ning, T.H. Press 1998. Fundamentals of modern VLSI Devices, Second edition, New York: Cambridge University, Reference to a chapter in an edited book: MOSFET Devices.
2. Hu, C. (1996, December). Gate oxide scaling limits and projection. In *International Electron Devices Meeting* (pp. 319-322).
3. Pal, R. S., Sharma, S., & Dasgupta, S. (2017, March). Recent trend of FinFET devices and its challenges: A review. In *2017 Conference on Emerging Devices and Smart Systems (ICEDSS)* (pp. 150-154). IEEE.
4. Wikipedia, FinFET.
5. Wong, H. S., Frank, D. J., & Solomon, P. M. (1998, December). Device design considerations for double-gate, ground-plane, and single-gated ultra-thin SOI MOSFET's at the 25 nm channel length generation. In *International Electron Devices Meeting 1998. Technical Digest (Cat. No. 98CH36217)* (pp. 407-410). IEEE.
6. Auth, C. (2012, September). 22-nm fully-depleted tri-gate CMOS transistors. In *Proceedings of the IEEE 2012 Custom Integrated Circuits Conference* (pp. 1-6). IEEE.
7. Rajprabu, R., Arun Raj, V., & Rajnarayanan, R. (2013). Performance Analysis of CMOS and FinFET Logic. IOSR Journal of VLSI and Signal Processing (IOSR-JVSP), 2(1), 1-6.
8. Arora, S., Dutta, U., & Sharma, V. K. A Noise Tolerant and Low Power Dynamic Logic Circuit Using Finfet Technology.
9. Subramanian, V. (2010). Multiple gate field-effect transistors for future CMOS technologies. *IETE Technical review*, *27*(6), 446-454.
10. Bhattacharya, D., & Jha, N. K. (2014). FinFETs: From devices to architectures. *Advances in Electronics*, *2014*.
11. Alioto, M. (2010). Comparative evaluation of layout density in 3T, 4T, and MT FinFET standard cells. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *19*(5), 751-762.
12. Jurczak, M., Collaert, N., Veloso, A., Hoffmann, T., & Biesemans, S. (2009, October). Review of FINFET technology. In *2009 Ieee International Soi Conference* (pp. 1-4). IEEE.
13. Duffy, R., & Shayesteh, M. (2011, January). FinFET doping; material science, metrology, and process modeling studies for optimized device performance. In *AIP Conference Proceedings* (Vol. 1321, No. 1, pp. 17-22). AIP.