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Study on Leakage Current Reduction Technique in VLSI Design

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Abstract

Designing of low-power circuit has become a very significant and difficult job in the current Microelectronics domain. Low power devices are the need of present electronics industries. In VLSI circuit design, power dissipation and leakage power present are the critical design constraints as they play a vital role to have a longer battery life (which is highly desirable!). On Chip Designing of Power management is one of the major challenges. Leakage power becomes a crucial parameter as the technology shrinks, for instance as we reduce the channel length from 180 nanometer to 90 nanometer or to 45 nanometers, controlling the effects of leakage power becomes more and more difficult. As the technology shrinks for a high-speed application higher voltage is required by the circuit to maintain the higher speed of operation which increase the amount of leakage in the circuit, numerous techniques have been proposed for leakage reduction in CMOS digital integrated circuit. This review article shows the multiple CMOS integrated circuit reduction techniques.

Keywords: VLSI, CMOS, GIDL, DIBL, VGS, TOX, FET, MOX, MTCMOS.

Research Article

1. Introduction

Need for low-power VLSI design is growing quickly every day, this is because the designers are upgrading circuit functionality within the single chip thereby increasing the energy demand per unit Area (Fig. 1). Hence, with the use of latest hostile scaling technology development, leakage energy minimization plays an essential role in current CMOS technology. A detailed introduction has been provided to the increasingly important leakage effect in the latest upcoming technologies with short channel devices. The main sources of leakage are of the sub-threshold leakage and door leakage. In future technologies leakage will dominate power hence we also analyze leakage optimization techniques and leakage appraisal approaches supporting optimization especially at basic abstract level [5].

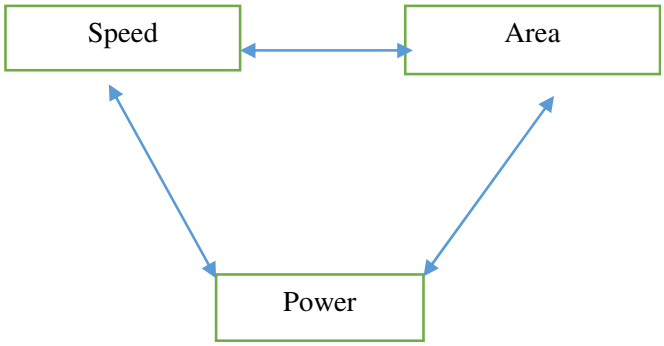


Figure 1 Relation among speed, area and power in low power VLSI

Figure 2 below shows a pn junction formation in a typical MOSFET.

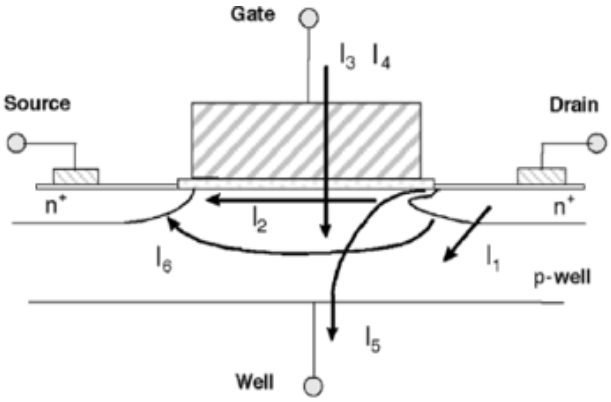


Figure 2 Summary of profound sub-micrometer transistor leakage present mechanism courtesy to reference [5].

1.1 Leakage*:* Leakage current occurs as a natural marvel of the semiconductor device action. A leakage is a form of current that is usually not envisioned for the normal operation of a digital circuit [3]. Ingestion of leakage energy plays a major role in present CMOS technology. We gave an introduction to the gradually important effect of the leakage in latest and imminent machineries and short channel devices.

A deep submicron CMOS transistor leakage current comprises of three main processes: junction tunneling, sub-threshold, and door tunneling currents as shown in Fig.3.

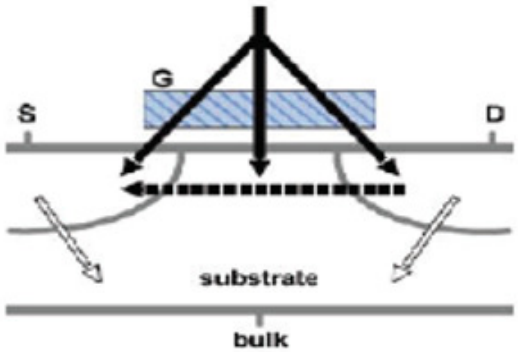


Figure 3 Different leakage mechanisms [courtesy to reference 5].

1.1.1. Subthreshold leakage: *Subthreshold leakage current* (Isub) in metal oxide semiconductor transistor occur whenever the applied gate voltage is less than the actual threshold voltage [6].

$$I_0=\mu C_{0x}(W/L)(kT/q)^2e^{1.8} \quad (1)$$

where,

μ0: Mobility zero prejudice,

Cox: Capacity of the gate oxide, and

(W / L) means the width of the leaky metal oxide semiconductor length ratio.

The variable V in equation (1) is the thermal voltage constant, and Vgs represents the gate to the source voltage, this is diffusion type of current [7] the total leakage during the off state is mainly dominated by this sub-threshold leakage. This phenomenon DIBL also called as drain induced barrier lowering occur due to application of high voltage in MOSFET with very small channel length, due to this phenomenon channel is formed by injection of charges from the source of the MOSFET which is independent of applied gate voltage. Very small width of MOSFET also changes the value of sub threshold current and the threshold voltage. Leakage current below threshold voltage is directly proportional to exponential of $(v_{gs}-v_t)$. Smaller channel result in smaller threshold voltage thereby increase the amount of sub-threshold leakage in the device.

1.1.2 Junction tunneling leakage

Junction leakage that effects the minority carrier diffusion and drifts near the edge of depletion regions, as well as the cohort of electron-hole pairs in reverse-bias junction depletion regions. There is also junction leakage due to band-to-band tunneling (BTBT) when both n regions and p regions areas are deeply doped, as is the case for chosen

progressive MOSFETs [4, 6]. Band-to-band tunneling Current: At high electrical field of around 10 V/cm electrons crosses the reverse-biased PN junction causing notable amount of charge carriers to move through the intersection due to tunneling of electrons from the p region's valence band to the n region's conductive band, as shown in Figure 4. From Figure 4, it is clear that the general voltage drop crossways must be extra than the band gap for the tunneling to occur. Subsequently silicon is a semiconductor of in-direct band gap, the BTBT present in silicon involves the manufacturing concerns due to incidence of phonons. The current density of the tunneling is provided by ' E' [8].
Junction leakage occurs from the minority carrier diffusion and drifts close to the edge of depletion regions and moreover from a cohort of electron-hole pairs in the depletion regions of reverse-bias junctions.

$$J_{b\text{-}b}=A\ EV_{app}/E_g^{1/2}\exp(-B\ E_g^{3/2}/E)$$

$$A=(2m^*)^{1/2}q^3/4\pi h^2 \text{ and } B=4(2m^*)^{1/2}/3qh \quad (2)$$

There is a definite mass of electron from the equation (2) m*; eg is the energy-band gap; Vapp is the functional reverse bias; e is the electrical field at the junction; q is the electronic charge, and Planck's constant is 1⁄2*π times the electrical field at the intersection is provided by [9].

$$E=(2qN_aN_d(V_{app}+V_{bi})/\epsilon_{si}(N_a+N_d))^{1/2} \quad (3)$$

From the equation (3) Na and Nd are the p and n side doping, respectively; ϵsi is silicon permittivity, and Vbi is the built-in junction voltage.

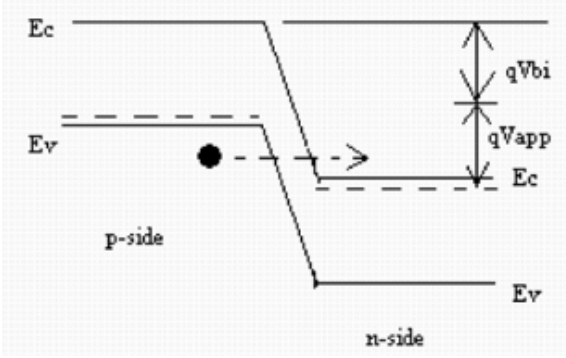


Figure 4 BTBT at the biased inverse pn junction [courtesy to reference 9].

In scaled devices, elevated attention to doping and unexpected doping describes the reason behind the drain-well intersection of significant BTBT current [4].

1.1.3 Gate tunneling leakage

The short channel CMOS device have low oxide thickness on application of high electric field causing tunneling of electron from substrate toward the MOS gate and vice versa. [6, 4], this phenomena of transfer of charges between gate and oxide on application of high electric field is referred as gate oxide tunneling [5].

$$I_{gate} = (A.C)\ (W.L)\ e^{-B\ tox/vgs\ \alpha}$$

Where, $A=q^3/8\pi h\varphi_b$, $B=8\pi(2m_{ox}\varphi_b^{3/2})/3hq$ and $C=(V_{gs}/t_{ox})^2$ (4)

From the equation 4, on the other hand, t_{ox} signify the thickness of gate oxide,I structure depends on the voltage drop across the oxide and ranges from 1 to 0.1, h isPlank's constant, φ_b is barrier height for electron/holes, m_{ox} is the actual mass of electron/holes [9,10].

2. Leakage reduction techniques

In CMOS nanoscale technology several methods are originated to overcome the problem of leakage in CMOS circuits [11].

2.1 Dual VT and MT CMOS

These methods are specified in [12,13], these were the initial methods used for the reduction of the leakage power in CMOS circuits.

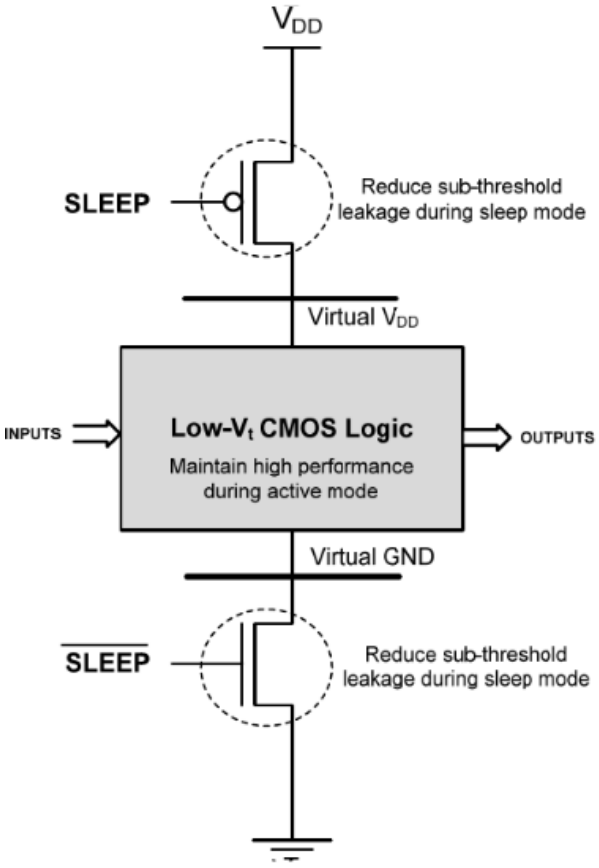


Figure 5 General MTCMOS circuit architecture [courtesy to reference 14].

There are many differences among DTCMOS and MTCMOS type of topologies, the gate in non-critical path uses high-threshold transistor and in the similarly critical path use the low threshold transistor. In the earlier method latency is natural and for dual technology this is much higher. The MTCMOS circuit diagram as shown in figure 5 have complicated structure making the manufacture procedure a very difficult task, both DTCMOS and MTCMOS method requires the supplementary mask layer of different widths for the each transistors to have different threshold, main difficulty in manufacturing variable V_T transistor is putting two different oxide thickness in a very small layout area [14].

2.2 Sleep mode approach

The approach to sleep mode was created to overwhelm the drawbacks of the method of dual VT and MTCMOS. According to [15] it is one of the most commonly known methods for sub-threshold leakage power reduction techniques. This method utilizes the sleep strategy and is one of the most frequently recognized outdated techniques for the decreasing of the sub-threshold leakage energy[15]. Additional transistors (sleep transistors) remain injected into the Power supply and Ground in this method [11].

- As described in [13], a "sleep" PMOS transistor is located between VDD and the circuit's pull-up network and a "sleep" NMOS transistor is located between the circuit's pull-down network and GND [16], by cutting off the power supports, these sleep transistors turn off the circuit. The sleep transistors are switched on when the circuit is dynamic and provide real low resistance in the transmission route so that the presence of the additional circuit element does not affect the normal mode of operation due to presence of these additional transistors. Using above described method the leakage energy in the circuit gets minimized through switched off

transistors which introduce great resistance in the route of leakage current during stand by or unused state of the circuit. Leakage power can therefore be effectively bridged by shutting off the energy biasing. Such techniques are called gated-VDD and gated-GND [11].

2.3 Sleepy keeper approach

According to Method suggested in [17], an added NMOS transistor is equal to the pull-up sleep transistor that relates VDD to the pull-up scheme. Subsequently the sleep transistor is off through sleep mode, this NMOS transistor is the VDD's only path for the pull-up scheme. An added solitary PMOS transistor is placed in the equivalent position of the pull-down sleep transistor that creates the path for pull-down network's only source to GND. The value of' 0' or '1' can be maintained in sleep mode, provide that the '0' or '1' worth has pre-sleep mode. This technique uses the output value of '0' or ' 1' for a GND-linked PMOS transistor to maintain output equivalent to '0' or a VDD-linked NMOS transistor to maintain output equivalent to '1' in sleep mode [14].

2.4 Transistor Stacking

The sub-threshold leakage current flow found in sequentially connected transistors is compact when turned off at the smallest node voltage. For instance, in Figure 6, elaborate the NAND gate scheme When M1 and M2 are mutually switched off, the voltage Vm between M1 and M2 at the transitional node is positive due to the small drain current. This has the following few impacts in the circuit's sub-threshold leakage flow, due to the favorable latent Vm the transistor M1 (0-Vm=-Vm) gate to source voltage becomes smaller followed by a reduced sub-threshold current.

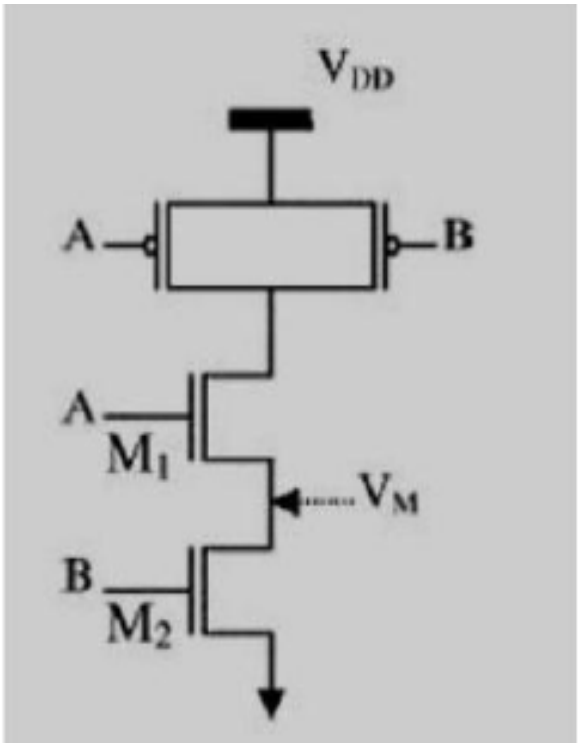
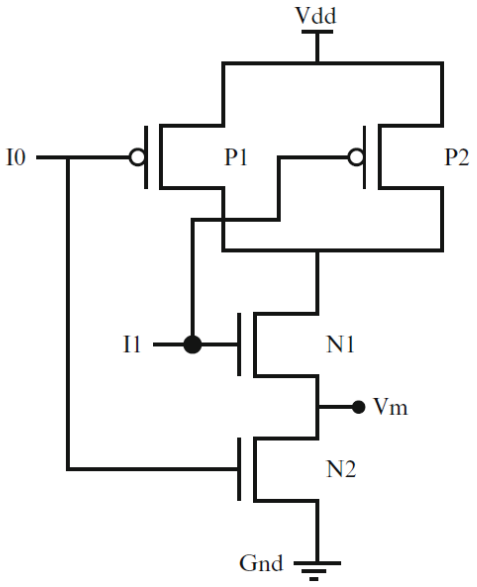


Figure 6 Two NAND gate input stacking impact [courtesy to reference 18].

Positive voltage Vm increase the M1 threshold voltage once again resulting in reduction of the leakage of the sub threshold current.

Classically, numerous gates may previously take tiny leakage due to the stacking effect in a huge circuit block, so one needs to apply collection of input vectors aiming to further reduce the leakage of an indolent circuit throughput on an input vector which offers lowest probable minor leakage current in the circuit [18].



Inputs (I0 I1)	Leakage
00	$2.I_{leak}$
01	I_{leak}
10	I_{leak}
11	~0

Figure 7 Several gates are inevitably stacked in the typical CMOS circuit and in a low leakage state. The problem with the low-leakage input vector discovery is to intervene the input that places most of the transistor in a low-leakage state.

2.5 Power Gating

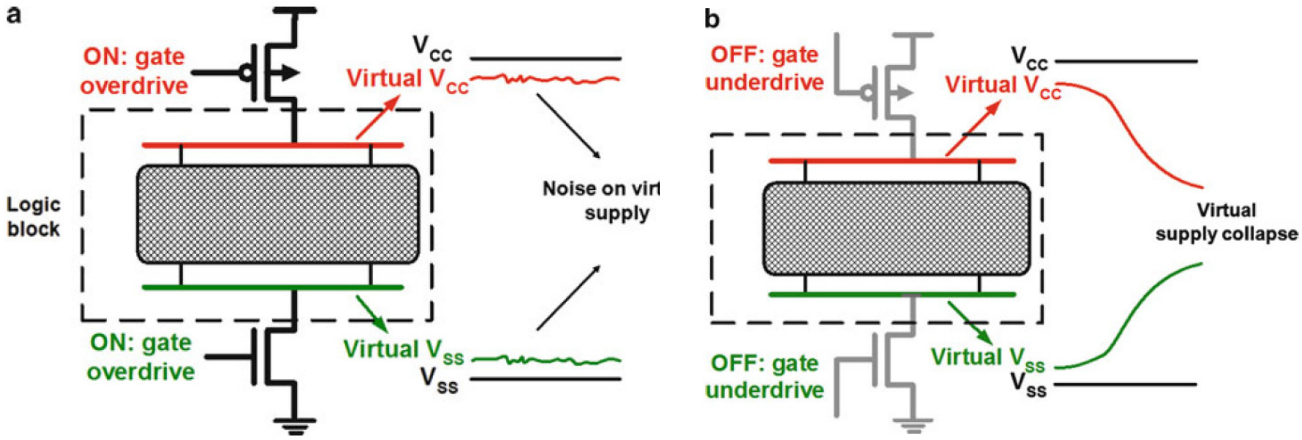


Figure 8 (a)Active mode: The circuit considers the virtual Vcc and virtual Vss that are very near to the Vcc and Vss respectively in the ' on ' state.(b) Ideal mode: Both the virtual Vcc and Vss are floating in the ' off ' state.

Power Gating is an active mechanism for lowering indolent circuit block leakage energy. In order to reduce the leakage energy, the power (Vdd) to circuit blocks that are not active are temporarily switched off. Once the block of the circuit becomes vital to the process, energy will again abound. The circuit block is not active during the current closure period, it is a low-power or inactive mode. The goal of power gating is therefore to minimize the leakage power by temporarily reducing the power to discriminate blocks that are not active. Power gating, as shown in Figure 8, is understood as a header switch by a pMOS transistor to shut

down the power supply to portions of a project in sleep mode. Using sleep transistors, the nMOS footnote switches are altered to be discarded. The implantation of the sleep transistors divides the energy scheme of the chip hooked on two components: a durable power [18].

2.6 Lector – Leakage Control Transistors

In the pull-up and pull-down scheme within the logic circuit shown in Figure 9, trendy LECTOR operation, dual leakage governor transistors (PMOS and NMOS) remain present [19]. These transistors are connected in such a way that the cut-off voltage for some input combination is continually closed by one of the transistors, increasing the track strength as a supply to the floor, prominent to a note worthy reduction in leakage currents. The mechanism of the LECTOR technique works together effectively in vigorous ways along with stand-in ways [14]. The circuit can be seen in the below figure.

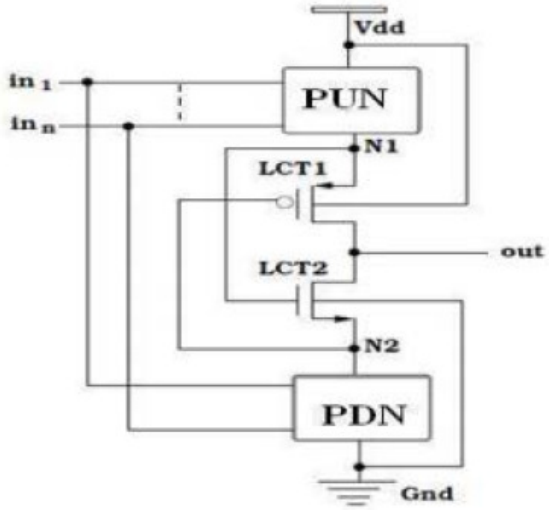


Figure 9 LECTOR design of the circuit [courtesy to reference 14]

They presented dual leakage control transistors (LCTs) in each CMOS gate so the basic notion behind this technique was the effective stacking of transistors in the supply voltage to ground pathways for shrinking leakage power. The authors in [15, 20, 21] and [22] have concluded commenting that "a state with extra transistor OFF in the supply voltage pathways to the ground is far less leakage than a state with solitary one transistor OFF in some supply to the ground pathway." Now their method that single LCTs are close to their cutoff section of the process. Here Leakage Control Transistor (LECTOR) technique was illustrated by the scenario of a NAND gate. A CMOS NAND gate with double-leakage transistor accumulation was proposed in reference [11].

3. Proposed mechanism

Till time various kinds of mechanism have been implemented and were quite impressively acceptable to overcome leakage issues.

3.1 In the 65nm technologies mutually the gate dielectric and subthreshold leakage currents necessarily be conditioned for minimizing power consumption through indolent and non-indolent manners. Thus, a new dominant method is planned for concurrently shrinking gate oxide and subthreshold leakage currents in domino logic circuits in the similar manner (ideal or non-ideal) with dissimilar input situations [6].

3.2 They developed a fast approach for computing total leakage current in large circuit blocks considering both subthreshold and gate tunneling currents. The proposed approach accurately accounts for the complex interaction between the stacked MOS configurations and is based on pre-

characterized tables of individual leakage currents for three distinct scenarios [23].

3.3 Power gating is a technique which is used to reduce the leakage power by shutting off the idle logic blocks using sleep transistors, they help in reducing the power, delay and switching time of the logic [24].

3.4 The leakage power reduction plays a vital role in low power VLSI circuit. The scrambling of a number of devices factors for improving the performance of VLSI systems but has added to the rise in leakage power dissipation. The current learning delivers a suitable choice for leakage power minimization method for a precise VLSI circuit founded on serial logical methodology. LECTOR method originates to be extra active in mutually inactive manner, LECTOR method is appropriate for earlier circuit process if propagation delay is the leading criteria [14].

3.5 By using our planned method, tentative consequences display equal to 70% reduction in the leakage current of combinational circuits be able to be attained at the expenditure of up to 15% interval consequence. We displayed in what way to transform the scan sequence of the circuit and use it to initiate the circuit with the least leakage vectors although the circuit is in stand-by mode. This efficiently removes the leakage overhead's by way of the vector-founded approaches [27].

3.6 With the constant increase in density of CMOS devices, the leakage current is playing a major role in the total power consumption. In current deep-sub-micrometer devices with low threshold voltages, subthreshold gate leakage too has converted governing foundations of leakage current and it rises with the technology scrambling. GIDL and BTBT might similarly develop a worry in progressive CMOS devices. To be able to decrease leakage in deep-submicrometer CMOS circuits, answers for this leakage minimization must be done at the procedure technology level and circuit stage level. As the progression technology innovates well-engineering methods through reversing and halo doping are used to decrease leakage progress short-channel features. At the circuit level, transistor stacking, many V_{th}, dynamic V_{th}, V_{dd}, and dynamic $V_{dd,}$ methods can efficiently shrink the leakage current in high-presentation logic and memory designs [4].

4. Motivation

Here are several methods which shrink power dissipation and help in low power applications, there is leakage power dissipation owing to the occurrence of threshold and gate channeling leakage currents. To minimize these leakages, dual threshold, MTCMOS, transistor stacking, sleep transistor methods are recycled, these methods will decrease extra leakage in the circuit. In today's domain, the rise of compactness of Integrated Circuits resulting an exponential growth in the manufacturing progression of VLSI circuits. The aspect of CMOS embedded circuits is daily attenuated for the compatibility with Deep submicron technology circuits. Thus, energy dissipation is a major issue for tiny network systems and sophisticated energy usage is major issue faced by digital embedded circuits in low power applications. Scrambling also leads to a higher process speed and advances the device performance. Reduced threshold voltage and

gate oxide also gives rise to the leakage current. In the direction of decreasing the leakage current we use the numerous methods as remarked in this paper, It must be noted that the double threshold technique decreases additional leakage current as compared to other methods discussed. For sinking the leakage current we also shrink the power dissipation in the circuit owing to which high temperature dissipation takes place in the circuit.

- MTCMOS approach is to use high-threshold voltage devices on non-critical processes in order to reduce the leakage energy using low-threshold devices on critical pathways in order to reduce the circuit power dissipation. This technique was called CMOS dual-threshold. Dual-threshold-CMOS is an identical active methodology for leakage reduction in mutually active manner and in stand-by manner. Process for about 80% of leakage power savings have been described in this paper. Dual-threshold CMOS is extensively used in present CMOS manufacture lines.
- It is realized that it is mostly due to sub-threshold leakage there is increase in complete leakage power of the circuit. In addition, leakage of gate-oxide is an additional likely aggressor for leakage power. A widely considered reasonable outcome is the prospective use of high-k (high dielectric constant) gate insulators.

Conclusion

In present time major concern today is leakage current in VLSI circuits

- Subthreshold leakage remains an issue, power gating is widespread in the thin oxide gate MOSFETs and leakage increases as the channel length is reduced.
- Hot carriers may become important carriers. If VDD does not preserve a level with technology, then dynamic and static energy in design need to be strikingly matched to decrease energy.
- Power savings and recycling will remain dominant subjects for the future.

Conflict of Interest

- The authors declare no conflict of interest.

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