



## A Review Article on Carbon Nanotube Field Effect Transistors Technology

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Received July 15, 2019; received in revised from July 26, 2019; Accepted July 26, 2019 Available online July, 2019

### Abstract

As Silicon industry is evolving it is scaling down day by day. With the reduced size of the transistor, the craving for high performance devices has also taken place. For MOSFET, with very small channel length size reduction is limited and below certain dimensions the device will undergo uncontrolled and unpredictable leakage current, parasitic capacitances and power dissipation issues. Hence, researchers have implemented a novel device to overcome the above-mentioned issues called as CNTFET (Carbon NanoTube Field Effect Transistor). CNTFET provides high carrier mobility, reduced delay and power consumption, better noise margin, suitable contact resistance and fast switching speed. In this review paper, different CNTFET structures and classifications, chiral vector and chirality have been discussed in detail.

**Keywords:** CNTFET, SCE, MOSFET, CNT, Chirality.

### 1. Introduction

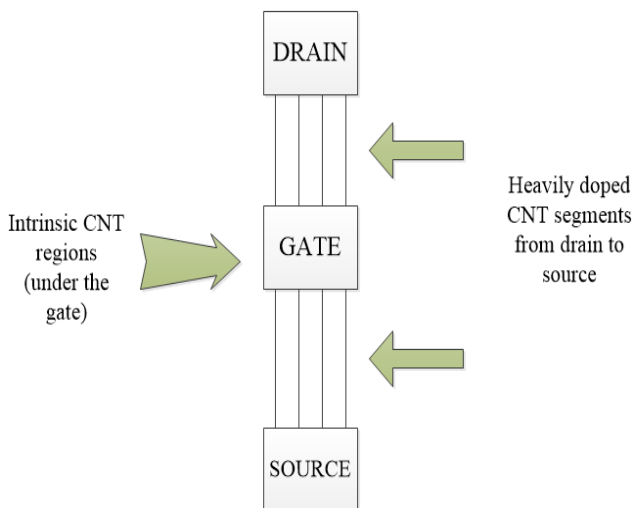
Moore's law says the number of transistors in an integrated circuit increases by the factor of two in every two years. This increment of transistors density requires smaller transistor sizing and to fulfill this transistor geometry has to be scaled down [1]. As transistor size is scaled down the transistor loses controllability of Gate over channel bringing Short Channel Effects (SCEs) into picture [2]. To overcome this and to increase the Gate controllability over the channel, a transistor having fin like structure has been introduced and is called as Fin Field Effect Transistor (FinFET). But it is very difficult and expensive to fabricate a multi gate FinFET with high accuracy, so we have to switch to another type of FET called as CNTFET. CNTFETs are considered as better FETs than FinFET because of its desirable electrical properties [3].

CNTFET is a Field Effect Transistor whose channel is assembled by using a single or several carbon nanotubes in between source and drain in a MOSFET structure [4]. Use of CNTs is an alternative replacement to silicon channel MOSFETS as channel of CNTFETs have more advanced electrical properties as compared to classical MOSFETs [5]. By replacing MOSFET from CNTFET, a superior drive current density can be achieved due to higher current carrier mobility in the latter [6]. Both the FETs (MOSFET and CNTFET) uses complementary (p-type and n-type) transistors [7], both transistors can be implemented by using nanotubes. To enhance the miniaturization of transistors, we switch to CNTFET, it overcomes noise problem and offers large Mean Free Path (MFP), smaller off-current, due to which the power dissipation is reduced and better performance over nanoscale electronics is achieved [3] and is an

advanced technique as compared to FinFET. Present article provides detail discussion on CNTFET Technology.

**2. Process Technology**

Here, a detailed description of various CNTFETs and their structures are discussed. CNTFETs are generally implemented by single carbon nanotube (named as Single-Walled Carbon NanoTubes, SWCNTs) or multiple carbon nanotubes (named Multi-Walled Carbon NanoTubes, MWCNTs) [8]. The nanotubes are designed by using a graphene sheet (called carbon ribbon), which is then rolled up in a cylindrical shape having the diameter of order of nanometer which varies from 0.6 to about 3 nanometers [9]. The graphene sheet can be rolled in different patterns following the desired functionality [9]. There are many advantages of SWCNTs and they are (a) high mobility for both electrons and holes, (b) ability to carry high current (around 10 micro A/ square nanometer) [10, 8].



**Figure 1 Schematic Diagram of a CNTFET Device (Top View)**

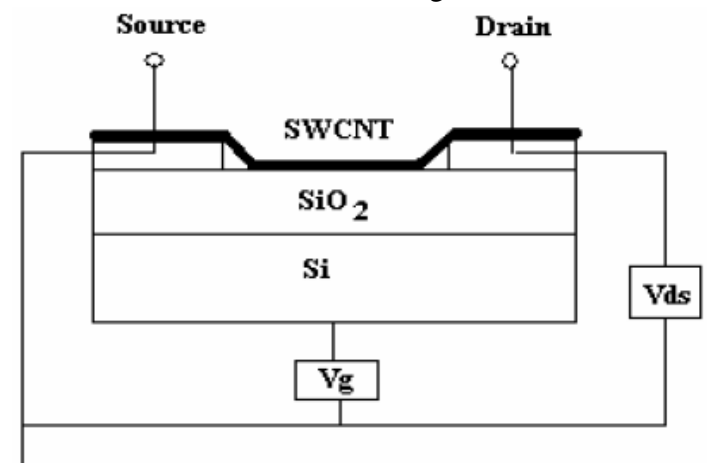
It also has superlative thermal, mechanical and electrical properties, due to which it became an

essential element for nanoelectronics device design [11]. Generally, the breadth and length of SWCNTs must vary from 1 to 2 nanometers and 100 to 10 micrometers, respectively [12]. Figure 1 shows a schematic diagram of CNTFET device (from top). Same design is also shown in paper [11].

Similar to the MOSFET devices, CNTFETs also have three terminals and they are: source, gate and drain (as shown in Figure 1). Current is allowed to transmit from source to drain through a channel during the on-state of gate [5]. The suburb between drain/source and gate is heavily doped to authorize low resistance during on state of gate [13].

**2.1 Device Fabrications**

**2.1.1 Back-gated CNTFET:** The back-gate CNTFET structure is shown in Figure 2.



**Figure 2 Back-gated CNTFET [Courtesy to Reference 10].**

In this structure, a Single Walled CNT has been used as a channel, through which the current can conduct, and is fabricated through lithography technique on an oxidized Si wafer [10]. In the figure, the two electrodes shown are behaving as source and drain, and heavily doped Si behaves as its back gate (Vg). This FET functions as p-type transistor whose

I(on)/I(off) ratio is around 10 seconds [10]. There are various demerits of this type of CNTFET such as (a) it has very low trans conductance (gm), (b) has low drive currents, (c) large parasitic contact resistances. To overcome these issues, a more advanced CNTFET, namely Top-gated CNTFET has been introduced [10].

**2.1.2 Top-gated CNTFET**

The top-gated CNTFET structure is shown in Figure 3.

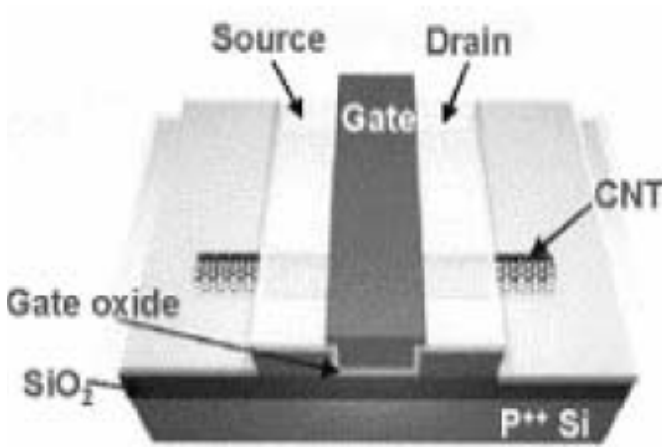


Figure 3 Top-gated CNTFET [Courtesy to Reference 10]

Table 1 Comparison between Top-gated and Back-gated CNTFETs

Parameters	Top-gated CNTFET	Back-gated CNTFET
Drain current	Microampere [10].	Nanoampere [10].
I(on)/I(off)	10 <sup>6</sup> [10]	10 <sup>5</sup> [10]
Threshold voltage	-0.5V [10]	-12V [10]
Transconductance (gm)	3.3 microseconds [10]	1 nanoseconds [10]

This CNTFET is advanced from Back-gated CNTFET, with Titanium (Ti) material gate, drain and source electrodes. In this CNTFET, the gate is fabricated upon the carbon tube and

15 nanometers silicon dioxide layer is fabricated as a gate oxide [10]. The comparison table (in Table 1) below illustrates the merits of Top-gated CNTFETs over Back-gated CNTFETs.

**2.2 Classifications**

The CNTFETs are classified in basically three categories:

- (i) Schottky-Barrier CNTFET (SB-CNTFET)
- (ii) Partially Gated (PG-CNTFET)
- (iii) Doped-Source/Drain CNTFET

Figure 4 shows the structures of all three possible types of CNTFETs. Let us know more about these CNTFETs in below sections.

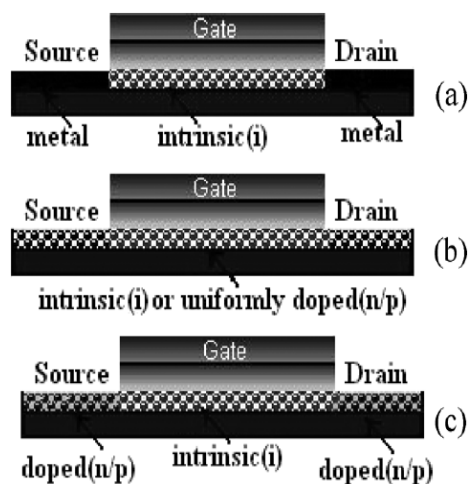


Figure 4 Three types of CNTFETs. (i) SB. (ii) PG. (iii) Doped-Source/Drain transistors [Courtesy to Reference [14]

**2.2.1 SB-CNTFET**

As shown in Figure 4, SB-CNTFETs used an intrinsic CNT as its channel [10]. The Schottky Barriers (SB) are formed by connecting the channel to source/drain [10]. These FETs are utilized as unfamiliar Schottky barrier FETs in which transistor behavior contrasts by varying contact resistance instead of channel conductance [10] and it manifests unbreakable ambipolar behavior, which degrades the use of

CNTFETs in CMOS like families [15]. This FET needs an accurate adjustment of SB and gate electrode [10]. It also decreases the ON-current of the devices [10]. To overcome this challenge, one has to switch to another type of CNTFET, described in below section.

**2.2.2 PG-CNTFET**

In this CNTFET, the nanotube is uniformly intrinsic or uniformly doped having some ohmic contacts at their ends and can be a p-type or n-type, when p-doped or n-doped respectively [14] these CNTFETs can function in depletion mode (uniformly p/n doped) [14] and is shown in Figure 4.

**2.2.3 Doped-Source/Drain CNTFET**

The structure is shown in Figure 4. These CNTFETs are collected by two un-gated sections that are lightly or heavily p/n doped [14].

**Table 2 Comparison between SB-CNTFET, PG-CNTFET and Doped-Source/Drain CNTFET**

Parameters	SB-CNTFET	PG-CNTFE T	Doped-S/D CNTFET
Dielectric	ZnO <sub>2</sub>	Al <sub>2</sub> O <sub>3</sub>	HfO <sub>2</sub>
Tox (nm)	15	4	8
Diameter (d)	Nearly about 1.4 nm	Nearly about 1.4 nm	Nearly about 1.6 nm
Tube length	260nm	600nm	80nm
Ion (microA/micrometer)	535	71	2500
Source/drain metal	Titanium	Titanium	Palladium
Gate position	top	Local	Top
V <sub>ds</sub>   (V)	0.5	0.5	0.5
Ion/I <sub>off</sub>	10 <sup>4</sup>	10 <sup>4</sup>	10 <sup>6</sup>

These can be functioned in pure p- or n-type depletion mode [16] or in enhancement mode

[17] that depends on the barrier’s height modulation principle [14]. Table 2 illustrates the comparison between these three CNTFETs.

**2.3 Chirality and chiral vectors**

As discussed earlier, CNTFETs are designed by using graphene sheets (also called nano ribbons). By rolling this graphene sheet, Carbon Nano Tube (CNT) can be implemented [17]. Due to its structural and electrostatic features, CNTFETs becomes more useful due to its feasible nanoelectronics features [18].

The CNT may have metallic or semiconductor behavior depending upon its parameter named chirality [9]. The metallic or semiconductor behavior of CNT can be defined by the angle in and direction into which a graphene sheet is rolled to form a tube [19]. Chirality is a geometric property of some ions or molecules [20]. There are two types of nanotube patterns (a) zigzag and (b) armchair [9]. Both patterns describe different types of carbon nanotubes depending upon how the sheet is rolled on [9]. Chirality can be understood by its chiral vectors (n, m). When both the vectors are equal (i.e., n = m), the nanotube is armchair and when m = 0, the nanotube is zigzag [21]. The metallic and semiconducting behavior of nanotube is also depending on its chiral vectors [21]. If n-m is non-divisible by 3, then the tube will act as semiconductor, otherwise it will act as metal [21]. To fulfill this condition, one-third of the tube must act as metal and two-third must act as semiconductor [21].

**3. Problem Identification**

Here, some drawbacks of CNTFET are discussed and are follows:

(a) Self heating: As we have seen, CNTFETs have CNTs as their channel, so the tubes are so concentrated that it can eliminate leakage

current, but it can face a self heating issue [4]. The charges can't be discharged, so it will heat up inside the tube itself and that can cause heat dissipation [4]. CNTs can be metallic or semiconductor, semiconductor CNTs dissipate less heat as compared to metallic CNTs [4].

(b) Apart from above advancements, few issues like hysteresis, high-density degradation issues, cost minimization are still unsolved [22].

(c) Shorter Lifetime: CNTs are made of carbon and this can be mortified when exposed to oxygen, so there is requirement of improvement to protect the CNT which can be achieved by introducing a new polymer material [4].

(d) CNTFETs are used to eliminate power dissipation and leakage current, but they have small power handling capacity [22].

(e) Reliability: Since CNTs are non reliable under high temperature and electric field. The joule breakdown results for metallic CNTs and avalanche breakdown results in case of semiconductor CNT [4].

(f) CNTFETs are expensive as compared to conventional CMOS devices and FinFETs [4].

#### 4. Future Scope

In this section, we have mentioned some possible improvements in recent CNTFET Technology.

- The cost effective CNTFET must be introduced as the recent one is very expensive because of its fabrication and manufacturing process [4].
- The measurability of CNTFETs must be explored in detail.
- New polymer and material must be introduced to extend the life time of CNTs [4].

- Issues occurring during placement of source and drain of FET must be resolved [4].
- Advanced methods must be introduced to eliminate breakdowns in both the cases (for semiconductor and metallic CNTs) [4].
- High reliability devices must be designed [4].

#### Conclusion

This article has presented detailed basic concepts of CNTFET applications in microelectronics. It eliminates various disadvantages of conventional bulk MOSFET by eliminate Short Channel Effects, power dissipation, leakage and is advantageous over complex structured FINFET (which is difficult to fabricate) by providing simple structure, higher noise margin, highly scaled small sized transistor thereby increasing transistor density in the chip. The drawbacks of CNTFET and some future scopes to overcome those demerits have been also discussed successfully.

#### Acknowledgment

The authors thanks to the reputed university Chhattisgarh Swami Vivekanand Technical University (CSVTU), Newai for providing golden opportunity for the successfully execution of the project work under the guidance of Mr. Prashant Dwivedi (HOD, Microelectronics and VLSI Department, UTD, CSVTU, Newai).

#### Conflict of Interest

The authors declare no conflict of interest.

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