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A Survey on ESD protection design in different RF circuits

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Abstract

ESD (electrostatic discharge) protection circuits are always needed in any of the RF (Radio Frequency) circuits to protect the circuit from electrostatic discharge. There are different types of ESD protection circuits. It is very important to protect the circuit from CMOS (Complementary metal oxide semi conductor) devices. In this review process we have discussed ESD protection design in different RF circuits following different recent articles. Present article contains useful information about the causes of ESD, problems arising due to ESD and useful solutions derived by various researchers.

Keywords: ESD, RF circuits, RF, IC, CMOS, I/O Pad, HBM, CDM.

Research Article

1. Introduction

Electrostatic discharge (ESD) is quick charge interaction between two points at different potentials. Discharge happens at very high speed between electrically charged objects if they suddenly come in direct contact due to electrical short or in case of breakdown of materials [1]. There is a little lightning due to collision of differently charged objects. ESD can create amazing lightning which is sometimes never seen but it is very abundant that can set off damage to electronic components. Types of discharges are corona discharge produced from sharp electrodes & brush discharge from blunt electrodes [2]. It can be harmful in industry like explosion in gas, fuel vapors and cold dust also there is failure in solid state components like IC (integrated circuit). They can also go through life time damage when given high voltages [3, 4]. These are some of the reasons which made researchers to pay attention to work towards it and manufactures to develop electrostatic protective areas.

2. Different Technology of ESD Protection

2.1 At various Frequency

To ensure ultra-high data rate applications credited to continuous dimension reduction and enhanced Radio Frequency (RF) performance, scaled silicon-on-isolation (SOI) CMOS technologies are commonly used for mm-wave ICs to attain low power, low costs and high integration. RF switches are building blocks for RF front end (RFFE) ICs, involving low insertion loss, high isolation and high power-handling potential. Series-shunt type SPDT RF switches of 28GHz and series-only SPDT switches at 38GHz with ESD protection were designed and fabricated as shown in Fig. 1 [4].

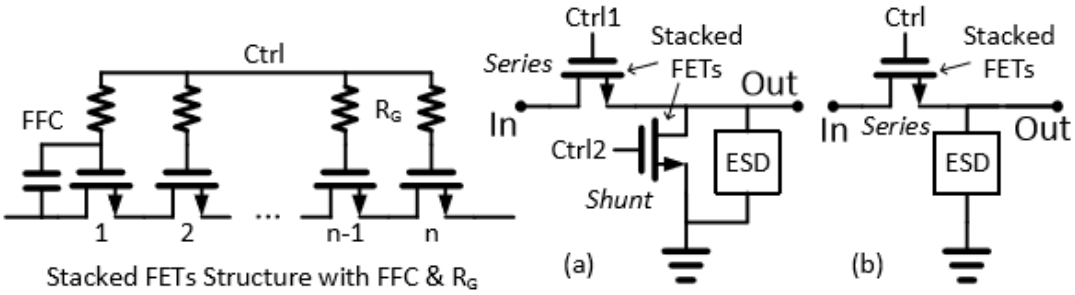

Figure 1 Series-shunt (a) and series-only (b) switch topologies feature stacked MOSFETs with output ESD protection [4]

Table 1 Summary of the design split data for the series and shunt MOSFET stacks

Design	Branch	FET Stack Number	Fingre Width (UM)	FIMGRE Number	Total Width (UM)	Gate Resistance (OHM)	FFC
28GHZ SPDT	SERIES	10	2.508	140	351.12	1K	20
	SHUNT	10	2.508	60	150.48	1.4K	20
38GHZ SPDT	SERIES	10	2.508	140	361.12	800	20

The transient voltage across the conventional LC tank ESD protection circuit must be reduced to improve ESD toughness of the RF circuits, especially for the circuits realized in nano scale CMOS technology. Therefore, a new modified LC-Tank ESD protection design is proposed by Chun-Yu. For 60-GHz RF applications ESD protection circuit has been designed and proposed in this article.

The LC-tanks are designed to reverberate for "open circuit" at the operating frequency of the RF circuit (Fig. 2). Thus, the parasitic effects of ESD diodes (DP and DN) will be isolated. The modified LC-tank ESD protection design has been verified to achieve the required 2kV - Human Body Model (HBM) ESD robustness with the lower power loss and smaller layout area [5].

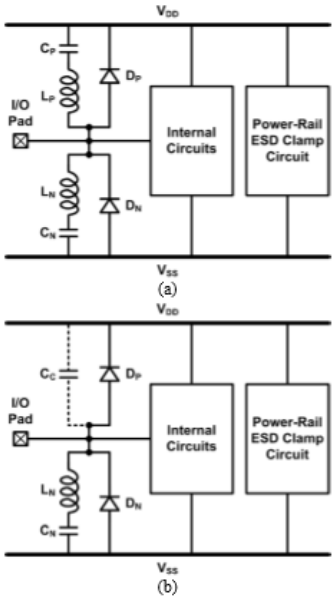

Figure 2 Modified LC-tank ESD protection design in RF circuits with (a) a pair of inductors and (b) only one inductor [5]

Design of ESD Protection for Large Signal Swing RF Inputs Operating to 24GHz in 0.18mm SiGe Bi CMOS Process by Srivatsan Parthasarathy [6] (Fig. 3). The performance deprivation resulting from the addition of ESD protection devices to very high-speed Analog/RF designs is the main cause for low ESD toughness in these applications. This paper introduces an ESD method that combines device development and characterization as well as simulation, for high speed Analog/RF products. In this work a special ground referenced ESD network is introduced for protecting RF ports with asymmetrical signal swings in the range of +3.5V/-3.5V operating from 6-24GHz [6].

A probable gain as well as ultrahigh isolation in RF switch circuit in 0.18um bicmos technology is established. The RF switch attains an ultrahigh isolation by cancelling of RF leaking technique in which it is restrained by combining its duplication using balun. As compare to convention switch topology its isolation is higher. RF switches such as SPST and T/R switches, etc can be used for higher isolations in the microwave and millimeter-wave regions [7].

The UWB which is also known as ulta-wideb and for radio communication it is one of the technologies for transmitting and receiving short, information–encoded, electromagnetic impulses. The proposed LNA is designed using single-stage cascade topologies. This circuit includes the bias network which has a power consumption of 49mW [8].

2.2 Variation of Technology

Li-Wei Chu [9] proposed the compacted and low-loss ESD protection designs for V-Band in 65-nm CMOS process. These ESD protection circuits are developed to support RF circuit designers for them to easily affect ESD protection. Such compact ESD protection circuits can attain the 2-kV HBM ESD toughness with 1.8-dB loss and small layout area. Fig. 3, the proposed design A can reduce the insertion loss at considered frequency band [9].

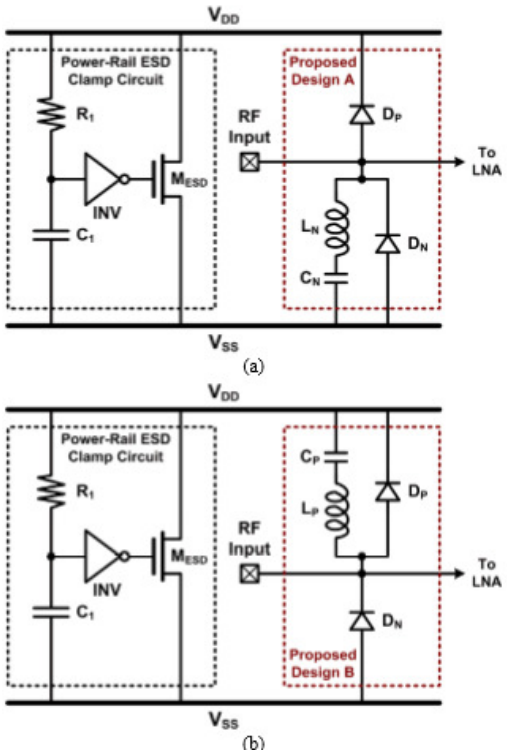

Figure 3 (a) Proposed ESD protection design A and (b) proposed ESD protection design B.

To reduce the inductance used in LN, another additional capacitor (CS) can be added to attach in parallel with ESD protection diode. In other words, the parasitic capacitance of ESD protection diodes (C Diodes) is increased by adding the parallel capacitor (CS). It is better to add the supplement capacitor rather than rising the diode size, because the additional capacitor provides the simply capacitance, while

increasing diode size lowers the parasitic resistance, which produces the lower parasitic impedance and higher insertion loss.

In ESD series –connected diode strings and protection diodes are used. As diodes are increased more and more the total extra noise figure of the diode string ESD protection is increased [10].

GGNMOS has low set off voltage and straightforward structure, therefore GGNMOS and GGNMOS triggered ESD protection devices are broadly used in ESD guard field. The impact of W on trigger voltage and holding voltage is mainly considered as well as the impact of L on holding voltage when designing GGNMOS under 40nm process [11].

Examination on various ESD protection strategies dedicated to 3.3V RF applications (2GHz) in a 0.18mm CMOS process by C. Richier, compares different ESD protection devices and shows that a appropriate ESD performance target for RF applications (200fF max, 2kV HBM) can be reached with a diode network method.

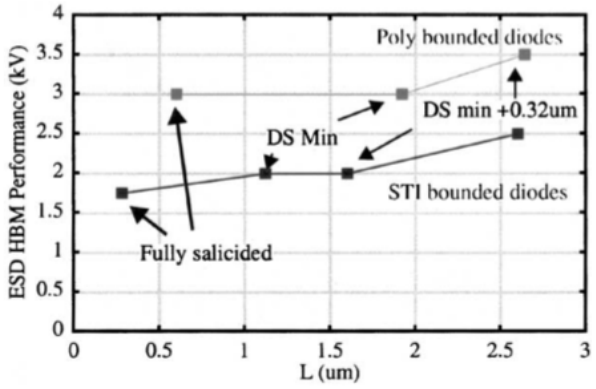

Figure 4 ESD performance of both STI and poly bounded N+/Pwell.

The optimization of the diodes is then a key point. A compromise has created between the ESD performance, the voltage drop during ESD and the parasitic capacitance. Poly as well as shallow trench isolation (STI) bounded diodes have been studied and it appears clearly that a solution based on poly bounded diodes is the best choice (Fig. 4). Different ESD protection strategies are offered and evaluated in terms of ESD performance but also in terms of parasitic capacitance.

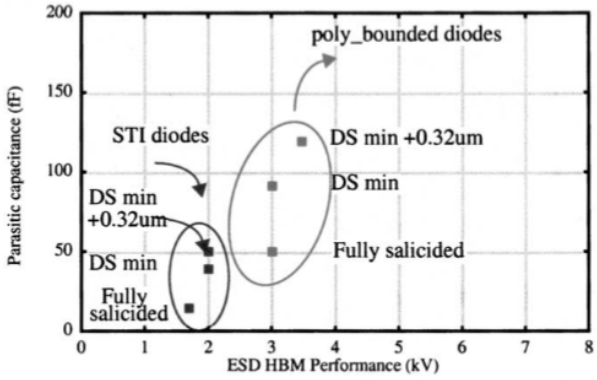

Figure 5 Maximum parasitic capacitance versus ESD performance for STI and polysilicon bounded diodes with various drain DS.

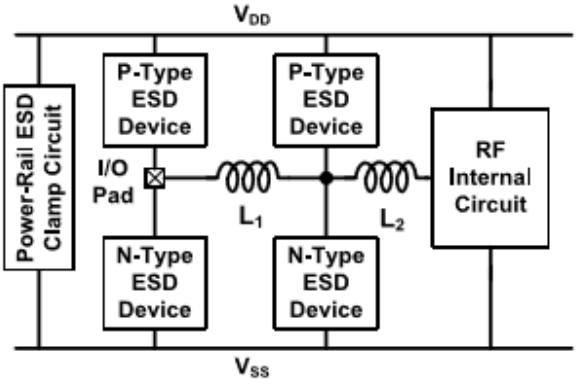

Figure 6 New proposed distributed ESD protection circuit with ESD devices in two stages for RF applications.

Poly and STI bounded diodes have been examined and poly diodes were found to have

the best trade-off for the safety of RF applications (Fig. 5) [12].

Chen [13] proposed a new distributed ESD protection structure with the stacked diodes with embedded silicon-controlled rectifier to achieve good ESD robustness without degrading the RF performance. The proposed ESD protection circuit was confirmed in a 40-nm, 2.5-V CMOS process to sustain a human-metal model of 5 kV (Fig. 6). The proposed ESD protection circuit is suitable to guard the broad band RF circuits in superior nano scale CMOS technology. This newly proposed protection circuit has achieved lower turn-ON resistance, good ESD robustness, and required RF performance.

Conclusion

The article contains reviews and found that for a preferred lower insertion loss, the switch isolation will become very poor, which limits the performance of a high frequency switch. In general, the ESD-induced parasitic effect, including resistance and capacitance from output to ground, increases the insertion loss in ON state, but improves the isolation in OFF state. The ESD protection circuit slightly degrades the RF gain of LNA. The insertion loss cannot be ideally 0 dB, since the parasitic resistance of ESD protection diodes (RDiodes), which cannot be eliminated by inductance, also loses the RF signals. Design of Low-Capacitance Electrostatic Discharge (ESD) Protection Devices in Advanced Silicon Technologies for high-speed designs, one need to think about lowering the HBM and CDM level further for Fin-FET technologies as ESD device capacitance loading becomes considerably higher while no improvement observed in Vt1 or It2 for FETs. A poor protection of the input-output pad as the voltage drop on the pad, which will be mainly given by the voltage drop across the diode, will become too high, leading to ESD damage in the input-output pad. Therefore, a two- or three-diode string may be optimal RF ESD protection solution due to balanced overall performance.

Conflict of interest

The authors declare no conflict of interest.

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